Remarks

In view of the above amendments to the claims and the following discussion, the applicants submit that none of the claims now pending in the application are obvious under the provisions of 35 U. S. C. § 103. Thus, the applicants believe that all of these claims are in allowable form.

REJECTIONS

A. 35 U. S. C. § 103

1. Claims 1-13 are not unpatentable over Bu

Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being obvious over Bu (U.S. Patent Publication 2002/0101172 published August 1, 2002). The applicants submit that these claims are not rendered obvious over this reference.

Claim 1 has been amended to better distinguish the present invention more clearly against the prior art. The definition of the current supply means have been shifted to lines 31-35 in amended claim 1 and includes in addition the subject matter "as soon as a modulator of each column is turned on", as disclosed in our US Publication US2008/272993A1: the power supply means is a DC voltage generator Vdd, see par. [0053] and figure 1, and "as soon as a modulator 14 of the column is turned on, by applying an address-and-select voltage, the corresponding emitter is supply by just the generator Vdd", par [0059]. This feature is also disclosed with regard to fig. 3D, which shows that the drain current Id flowing through modulator 14 and emitter 2 starts flowing at the same time when Idata is applied to the gate of modulator 14. The new subject matter "and for turning on the emitters already during the programming step", is disclosed in pars. [0091-0094]: during a programming step C, a drive current I_{data} is applied to the gate of modulator 14, which generates a drain current I_d flowing through the modulator 14 and correspondingly also through emitter 2, which

illuminates, par. [0094]. The emitters are therefore already turned on during the programming step C, as disclosed also in fig. 3D, which shows that the drain current I_d already starts flowing when drive current I_{data} is applied to the modulator 14.

The image display device as described by the new claim 1 operates as follows: during a step A, a voltage V_{select} is applied to switch 16 and a control unit 34, which provides in response a reset voltage V_{reset} to address electrode 10 to discharge capacitor 18, par [0089]. The emitter 2 is therefore switched off and modulator 14 and capacitor 18 are in a defined state. In a short intermediate step B, a dead time is created to separate the reset step from the programming step, to avoid any short circuit, par [0090].

During programming step C, a drive current I_{data} is applied to the gate of modulator 14 and capacitor 18, so that capacitor 18 is charged and a drain current I_d is flowing through modulator 14 and correspondingly through emitter 2. The emitter 2 is therefore supplied with power by generator Vdd already during the programming step C, par. [0094]. These steps are also clearly shown in figs. 3A-3D.

The drain current I_d flowing through emitter 2 is measured at the same time by a single separate unit 26, which comprises e.g. a resistor and a precision operational amplifier, as described with regard to figure 2 of the present invention application, par [0081], for providing a value representative of the drain current I_d, as supplied to the selected emitter 2. A comparator compares this representative value of the drain current I_d with the value representative of the data set point, voltage V_c, for controlling the quantity of charge stored in the storage capacitor 18. As can be seen with regard to figure 3D, the drain current I_d is rising until a current value is reached corresponding with drive current I_{data}, in which case comparator 28 provides a warning signal S to control unit 34, which in turn closes switch 32 to interrupt the drive current I_{data}, as shown in fig. 3D. The programming step C is therefore completed, par. [0096].

In the next step D, the select voltage V_{select} is switched off, fig. 3A, because in capacitor 18 now the correct drive I_{data} for modulator 14 stored, to continue to provide the correct drain current I_d to emitter 2 which continues therefore with light emission during an emission phase following the programming phase over the duration of an image frame, until in a further step a new step A is provided for resetting the address circuit 6 with capacitor 18, for providing a further programming step for a corresponding new frame, par. [0101].

The emitter 2 continues therefore illuminating with the correct drain current I_{data}, until a new reset step A is applied, as shown in fig. 3D, but is illuminating also already during programming step C. The correct drain current I_d is provided independently of the individual trip voltage of selected emitter 2, because the drain current I_d flowing through emitter 2 is measured during light emission by means of measuring unit 26 and comparator 28, and when the correct drive current I_{data} is applied to capacitor 18, corresponding with control voltage Uc, the respective drain current I_d is maintained. Therefore a very efficient trip-threshold compensation means is provided, including e.g. a measuring circuit 26 with a comparator 28 and only a simple resistor 45 in the supply line 4 of voltage generator Vdd, which measuring circuit 26 is operative for a complete column of the image display device, as described with regard to fig. 1, par [0068].

The cited reference Bu, US 6,433,488 B1, describes an image display device comprising a circuit block 5 with two transistors 53, 54 arranged in the supply line between an emitter 1 and a supply voltage generator providing supply voltage Vs. Transistor 54 is arranged in the supply line for interrupting the voltage supply to the emitter 1, and transistor 53 is arranged for applying at the same time a driving current I_{OLED} to emitter 1. The circuit block 5 includes further an inverter ahead of transistor 54, so that, when a scan signal is applied to circuit block 5, transistor 53 is switched through and transistor 54 is blocked, to apply only driving current I_{OLED} to emitter 1 during a programming mode.

A current comparator 6 compares driving current I_{OLED} with a reference current I_{REF} in the programming mode and provides a feedback voltage V_{FB} for a data signal at input 4, to compensate the trip-threshold voltage of modulator 21. When the driving current I_{OLED} is smaller than reference current I_{REF}, a positive feedback voltage V_{FB} is output so that the voltage at the gate electrode 213 of modulator 21 increases. Correspondingly, when the driving current I_{OLED} is larger than reference current I_{REF}, the voltage at the gate electrode 213 is decreased, column 3, line 64 – column 4, line 11. When the programming mode is finished, the scan signal 3 is turned to low, so that driving current I_{OLED} is switched off via transistor 53 and transistor 54 is switched on for supplying emitter 1 with supply voltage Vs for light emission, during an emission phase, col. 1, lines 62-64 and col. 4, lines 12-25. The emitters of the image display device of Bu provide therefore a uniform light emission of the complete array independently of an individual trip-threshold voltage of each emitter.

The reference Bu discloses therefore a programming phase, during which a specific drive current I_{OLED} is applied to emitter 1, for providing a correct programming voltage for modulator 21, and an emission phase, during which supply voltage Vs is provided to emitter 1, for providing a correct light emission of emitter 1. As described with regard to fig. 2, circuit block 5 is required for each emitter 1, to provide the correct programming voltage for the respective modulator 21, because when circuit block 5 would be used for a subsequent emitter of a row, the supply voltage Vs to the previous emitter would be interrupted by transistor 54.

The image display device as described by Bu is therefore completely different with regard to the image display device as described in the new claim 1:

> With the present invention, the emitter is already turned on during the programming step and continues to illuminate, during programming step and emission step, until a reset signal is provided for generating a new image frame.

Bu discloses an image display device comprising a programming step, in which current I_{OLED} is provided for emitter 1 for comparing the current I_{OLED} with reference current I_{ref}, and an emission phase, during which supply voltage Vs is connected to emitter 1 for providing light emission of emitter 1.

Bu therefore does not disclose:

"current supply means capable of supplying current simultaneously to all of the emitters of each column through a same and single supply line during both emission steps and programming steps of the emitters of said column, as soon as a modulator of each column is turned on", claim 1, lines 25 – 27, and

"for turning on the emitters already during the programming step", claim 1, line 38.

The present invention has the advantage that the emitter 2 provides already illuminating light during the programming phase and is not switched off after the programming phase, therefore continues to emit light, which provides a brighter picture display with regard to the image display device of Bu.

The present invention has the further advantage, that the only one voltage source Vdd is used for providing supply current for obtaining the correct programming voltage for modulator 14 during the programming phase as well as for providing supply current during the emission phase. No switching off of the supply current I_d is necessary after the programming phase, and therefore no additional switches have to be provided, which is the case for the image display device of Bu.

Because the reference Bu provides for each emitter 1 a respective drive current I_{OLED} for comparison with a reference current I_{REF}, each individual emitter 1 of Bu requires respective switches 53, 54, also an inverter INV, so that a high number of components is necessary, corresponding to the number of emitters 1 for the image display device of Bu. The voltage generator Vdd of the present

invention provides the drain current I_d to all emitters of a row via line 4, so that only a single unit 12 is necessary for a complete column of emitters 2. The number of circuit components is therefore essentially reduced with regard to the image display device of Bu.

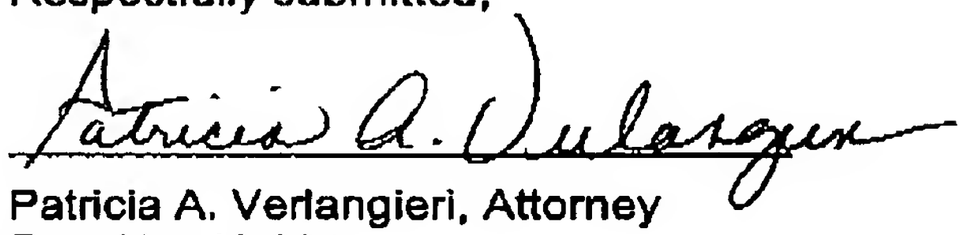
In view of the above arguments, Applicants respectfully submit that claim 1 is patentable over Bu and therefore, claims 2-13 are also patentable based on their dependence upon claim 1.

CONCLUSION

Thus, the applicants submit that none of the claims, presently in the application, are obvious under the provisions of 35 U. S. C. § 103. Consequently, the applicants believe that all of the claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Ms. Patricia A. Verlangieri, at (609) 734-6867, so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



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